IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BOARD OF PATENT APPEALS AND INTERFERENCES

In re patent application of:
Park, et al.

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For: METHOD TO PRODUCE TRANSISTOR HAVING REDUCED GATE HEIGHT

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APPELLANTS' APPEAL BRIEF

Sirs:

Appellant respectfully appeals the final rejection of claims 1-2, 4-9, 11-17, 19-24, and 26-28, in the Office Action dated August 29, 2006. A Notice of Appeal was timely filed on September 26, 2006.

Appeal Brief

I. REAL PARTY IN INTEREST

The real party in interest is International Business Machines Corporation, Armonk, New York, assignee of 100% interest of the above-referenced patent application.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, Appellants' legal representative or Assignee which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-2, 4-9, 11-17, 19-24, and 26-28 are all the claims pending in the application, are set forth fully in the attached appendix (Section IX), and are all under appeal. Claims 1-28 were originally filed in the application. A non-final Office Action was issued on May 3, 2005 rejecting claims 1-28. The Appellants filed an Amendent under 37 C.F.R. §1.111 on July 18, 2005 amending claims 1-5, 7-11, 13-19, 22-24, and 28.

A first final Office Action was issued on October 4, 2005 rejecting claims 1-28. The Appellants filed an Amendent under 37 C.F.R. §1.116 on November 30, 2005 amending claims 1, 3-4, 9-11, 16, 18-19, and 24. An Advisory Action was issued on

December 16, 2005 indicating that the Amendent filed under 37 C.F.R. §1.116 on November 30, 2005 would not be entered.

The Appellants filed a Request for Continued Examination and a Submission in Support of Request for Continued Examination amending claims 1, 4, 9, 11, 15-16, 19, 22, and 24 and cancelling claims 3, 10, 18, and 25. A non-final Office Action was issued on January 24, 2006 rejecting claims 1-2, 4-9, 11-17, 19-24, and 26-28. The Appellants filed an Amendent under 37 C.F.R. §1.111 on April 18, 2006 amending claims 1, 9, 16, and 24.

A second final Office Action was issued on July 5, 2006 rejecting claims 1-2, 4-9, 11-17, 19-24, and 26-28. The Appellants filed a response under 37 C.F.R. §1.116 on August 15, 2006 without amending the claims. An Advisory Action was issued on August 29, 2006 indicating that the proposed amendents (of which there were none) filed under 37 C.F.R. §1.116 on August 15, 2006 would not be entered and that "request for recondisderation, which has not been entered, does not clearly appear to overcome the rejections." Thus, the claims attached hereto are as of the April 18, 2006 amendment which was entered. The Appellants filed a timely Notice of Appeal on September 26, 2006.

Claims 1-2, 4-9, 11-17, 19-24, and 26-28 stand rejected under 35 U.S.C. §102(b) as being anticipated by Park, et al. (U.S. Patent No. 6,429,084), hereinafter referred to as Park. Appellants respectfully traverse these rejections based on the discussion in sections IV-VII below.

Appeal Brief

IV. STATEMENT OF AMENDMENTS

An final Office Action dated August 29, 2006 stated all the pending claims 1-2, 4-9, 11-17, 19-24, and 26-28 were rejected. The claims shown in the appendix (Section IX) are shown in their entered form as of the July 5, 2006 final rejection of the claims.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The Appellants' claimed invention is described in paragraphs [0007] through [0012] of the specification and shown in Figures 1A through 15B of the application as originally filed. More specifically:

Claim 1: A method of forming an integrated circuit transistor having a reduced gate height (paragraphs [0007], [0029], [0030], and [0049]) comprising:

forming a laminated structure having a substrate, a gate conductor above said substrate, and at least one sacrificial layer above said gate conductor; (paragraphs [0007] and [0033-0037] and Figures 1A-1B)

patterning said laminated structure into at least one gate stack extending from said substrate; (paragraphs [0007] and [0037] and Figures 2A-2B)

forming spacers with a target spacer width adjacent to said gate stack, (paragraphs [0008], [0012], [0029-0031] and [0040] and Figures 6A-6B)

wherein in order to achieve said target spacer width, a combined height of said gate conductor and said at least one sacrificial layer is predetermined; (paragraphs

Appeal Brief

[0008], [0029-0031], [0035-0036], [0039-0040] and [0050])

doping regions of said substrate not protected by said spacers with an impurity to form source and drain regions adjacent said gate stack (paragraph [0042] and Figures 7A-7B),

wherein said target spacer width is predetermined to ensure that said spacers sufficiently separate said source and drain regions from said gate stack so as to avoid lateral encroachment of said impurity into a channel region below said gate stack regardless of a height of said gate conductor; (paragraphs [0008], [0012], [0029], [0030]--which refers to the lateral encroachment problem discussed in paragraph [0005]), [0031], [0035-0036], [0039-0040] and [0050]) and

removing said spacers and said sacrificial layer (paragraph [0043] and Figures 8A-8B).

Claim 9: A method of forming an integrated circuit transistor having a reduced gate height (paragraphs [0007], [0029], [0030], and [0049]) comprising:

forming a laminated structure having a substrate, a gate conductor above said substrate, and at least one sacrificial layer above said gate conductor; (paragraphs [0007] and [0033-0037] and Figures 1A-1B)

patterning said laminated structure into at least one gate stack extending from said substrate; (paragraphs [0007] and [0037] and Figures 2A-2B)

forming spacers with a target spacer width adjacent to said gate, (paragraphs [0008], [0029-0031] and [0040] and Figures 6A-6B)

wherein in order to achieve said target spacer width, a combined height of said gate conductor and said at least one sacrificial layer is predetermined; (paragraphs [0008], [0029-0031], [0035-0036], [0039-0040] and [0050])

epitaxially growing raised source and drain regions on said substrate adjacent said spacers; (paragraph [0041] and Figures 7A-7B)

after said epitaxially growing of said raised source and drain regions, implanting an impurity into said raised source and drain regions and into said substrate below said raised source and drain regions (paragraph [0042] and Figures 7A-7B),

wherein implanting said impurity after said epitaxially growing of said raised source and drain regions avoids subjecting said impurity to the thermal budget of said epitaxially growing process (paragraph [0042]) and

wherein said target spacer width is predetermined to ensure that said spacers sufficiently separate said raised source and drain regions from said gate stack so as to avoid lateral encroachment of said impurity into a channel region below said gate stack regardless of a height of said gate conductor; (paragraphs [0008], [0029], [0030]--which refers to the lateral encroachment problem discussed in paragraph [0005]), [0031], [0035-0036], [0039-0040] and [0050]) and

removing said spacers and said sacrificial layer. (paragraph [0043] and Figures 8A-8B)

Claim 16: A method of forming an integrated circuit transistor having a reduced gate height (paragraphs [0007], [0029], [0030], and [0049]) comprising:

forming a laminated structure having a substrate, a gate conductor above said substrate, and at least one sacrificial layer above said gate conductor; (paragraphs [0007] and [0033-0037] and Figure 1B)

patterning said laminated structure into at least one gate stack extending from said substrate; (paragraphs [0007] and [0037] and Figure 2B)

forming spacers with a target spacer width adjacent to said gate stack, (paragraphs [0008], [0029-0031] and [0040] and Figure 3B)

wherein in order to achieve said target spacer width, a combined height of said gate conductor and said at least one sacrificial layer is predetermined; (paragraphs [0008], [0029-0031], [0035-0036], [0039-0040] and [0050])

epitaxially growing raised source and drain regions on said substrate adjacent said spacers, (paragraph [0041] and Figure 7B)

wherein said process of epitaxially growing said raised source and drain regions is performed in the absence of doping impurities (paragraphs [0031], [0036] 0041), and [0051] and p-type devices Figures 1B-7B which illustrate an absence of doping impurities in the device formation prior to eptiaxially growing the raised source and drain regions)

after said epitaxially growing of said raised source and drain regions, implanting an impurity into said raised source and drain regions and into said substrate below said raised source and drain regions, (paragraph [0042] and Figures 7A-7B),

wherein implanting said impurity after said epitaxially growing of said raised source and drain regions avoids subjecting said impurity to the thermal budget of

Appeal Brief

said epitaxially growing process (paragraphs [0042] and [0047]) and

wherein said target spacer width is predetermined to ensure that said spacers sufficiently separate said raised source and drain regions from said gate stack so as to avoid lateral encroachment of said impurity into a channel region below said gate stack regardless of a height of said gate conductor; (paragraphs [0008], [0029], [0030]--which refers to the lateral encroachment problem discussed in paragraph [0005]), [0031], [0035-0036], [0039-0040] and [0050]) and

removing said spacers and said sacrificial layer. (paragraph [0043] and Figures 8A-8B)

Claim 24: A method of producing an integrated circuit transistor (paragraphs [0007], [0029], [0030], and [0049]) comprising:

forming a laminated stack deposition (paragraphs [0007] and [0033-0037] and Figure 1B), wherein said laminated stack deposition is formed in a process comprising:

forming a silicon layer over a substrate layer; (paragraphs [0033] and [0034])

forming a gate oxide on said silicon layer; (paragraphs [0033] and [0035])

forming a gate conductor on said gate oxide; (paragraphs [0033] and [0035])

forming of least one sacrificial material above said gate conductor; (paragraphs [0033] and [0036]);

patterning said gate oxide, gate conductor, and said sacrificial material into at

Appeal Brief

least one gate stack; (paragraph [0037])

forming temporary spacers with a target spacer width adjacent to said gate stack, (paragraphs [0008], [0029-0031] and [0040] and Figure 3B)

wherein in order to achieve said target spacer width, a combined height of said gate conductor and said at least one sacrificial layer is predetermined; (paragraphs [0008], [0029-0031], [0035-0036], [0039-0040] and [0050])

epitaxially growing raised source and drain regions above said substrate layer adjacent said temporary spacers, such that said temporary spacers separate said raised source and drain regions from said gate stack, (paragraphs [0041] and [0050] and Figures 7B)

wherein said process of epitaxially growing said raised source and drain regions is performed in the absence of doping impurities; (paragraphs [0031], [0036] 0041), and [0051] and p-type devices Figures 1B-7B which illustrate an absence of doping impurities in the device formation prior to eptiaxially growing the raised source and drain regions)

simultaneously implanting an impurity into said raised source and drain regions and into said substrate below said raised source and drain regions, (paragraph [0042] and Figures 7A-7B])

wherein implanting said impurity after said epitaxially growing of said raised source and drain regions avoids subjecting said impurity to the thermal budget of said epitaxially growing process (paragraphs [0042] and [0047]) and

wherein said target spacer width is predetermined to ensure that said

temporary spacers sufficiently separate said raised source and drain regions from said gate stack so as to avoid lateral encroachment of said impurity into a channel region below said gate stack regardless of a height of said gate conductor; (paragraphs [0008], [0029], [0030]--which refers to the lateral encroachment problem discussed in paragraph [0005]), [0031], [0035-0036], [0039-0040] and [0050])

growing an additional dielectric layer on said raised source and drain regions; (paragraph [0043] and Figures 8A-8B)

removing said temporary spacers without removing all of said sacrificial material; (paragraph [0043]-[0044))

performing a halo implant in said raised source and drain regions and in exposed regions of said silicon layer; (paragraph [0044] and Figures 9A and 9B)

forming a permanent spacer adjacent said gate stack, wherein said permanent spacer is thinner than said temporary spacer; (paragraphs [0045] and Figures 11A and 11B)

performing a source and drain extensions implant in said raised source and drain regions and exposed regions of said silicon; (paragraph [0045] and Figures 11A and 11B)

forming a final spacer filling said exposed regions of said silicon between said permanent spacer and said raised source and drain regions; (paragraph [0046] and Figures 12A and 12B)

implanting additional impurities into said raised source and drain regions and exposed regions of said silicon; (paragraph [0052]))

annealing to activate all impurities; (paragraphs [0047] and [0052] and Figures

Appeal Brief

13A and 13B)

etching back said additional dielectric layer on said raised source and drain regions; (paragraph [0052]) and

saliciding both said gate conductor and said raised source and drain regions (paragraphs [0048] and [0052] and Figures 14A and 14B).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issues presented for review by the Board of Patents Appeals and Interferences are whether claims 1-2, 4-9, 11-17, 19-24, and 26-28 are unpatentable under 35 U.S.C. §102(b) as being anticipated by Park.

VII. ARGUMENT

A. The Prior Art Reference

Park teaches, in raised source/drain CMOS processing, the prior art problem of lateral epi growth on the gate stack interfering physically with the raised S/D structures and producing device characteristics that vary along the length of the gate and the problem of overetch of the STI oxide during the preclean step is solved by using a sacrificial nitride layer to block both the STI region and the gate stack, together with a process sequence in which the halo and extension implants are performed after the S/D implant anneal (see Abstract).

Appeal Brief

B. The Position In The Office Action Regarding The Prior Art Rejections

Claims 1-2, 4-9, 11-17, 19-24, and 26-28

Referring to claim 1, the Final Rejection suggests that Park discloses a method of forming an integrated circuit transistor having a reduced gate height, said method comprising: forming a laminated structure having a substrate (i.e., SOI substrate), a gate conductor (50) above the substrate (see Fig. 1), and at least one sacrificial layer (51 52 54) above the gate conductor (50); patterning the laminated structure into at least one gate stack (55) extending from the substrate (see Fig. 1) (Col. 1, lines 50-65); forming spacers (60 70) with a target spacer width adjacent to said gate stack (55) (see Fig. 2), wherein in order to achieve the target spacer width, a combined height of the gate conductor and the at least one sacrificial layer is predetermined; doping regions of the substrate not protected by the spacers (60 70) with an impurity to form source and drain regions adjacent the gate stack (55); wherein the spacers with the target spacer width is predetermined to ensure the spacers sufficiently separate the source drain regions form that gate stack so to avoid lateral encroachment of the impurity into a channel region below the gate stack regardless of a height of the gate conductor; and removing the spacers and the sacrificial layer (see Figs. 1-12 and related text Col. 1, line 50 - Col. 3, line 20).

Regarding claim 2, the Office Action suggests that Park discloses the method in claim 1, wherein forming of the spacers adjacent the gate stack comprises forming of the spacers adjacent the gate conductor and at least on sacrificial oxide layer (54) above the

Appeal Brief

gate conductor (50) (see Figs. 1-12 and related text Col. 1, line 50 - Col. 3, line 20).

Regarding claim 4, the Office Action suggests that Park discloses the method in claim 1, wherein the forming of comprises the spacers so as to positions the source and drain regions further from the gate conductor when compared to source and drain regions formed with spacers formed only to said height of said gate conductor (see Figs. 1-12 and related text Col. 1, line 50 - Col. 3, line 20).

Regarding claim 5, the Office Action suggests that Park discloses the method in claim 1, wherein said sacrificial layer above said gate conductor is formed in a process comprising: forming a sacrificial oxide layer above said gate conductor, and forming additional sacrificial layers above said oxide layer (see Figs. 1-12 and related text Col. 1, line 50 - Col. 3, line 20).

Regarding claim 6, the Office Action suggests that Park discloses the method of claim 1 wherein said sacrificial oxide layer protects said gate conductor (see Figs. 1-12 and related text Col. 1, line 50 - Col. 3, line 20).

Regarding claim 7, the Office Action suggests that Park discloses the method of claim 1 wherein said laminated structure includes a gate dielectric (40) below said gate conductor layer and a silicon layer (i.e., part of SQI) below said gate conductor (50), wherein said method further comprises doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process, wherein the combined height of said gate conductor and said sacrificial layer prevents said impurity from reaching said silicon layer, and whereas, without said sacrificial layer, said doping process would implant an impurity through said gate conductor and said gate

dielectric layer to said silicon layer (see Figs. 1-12 and related text Col. 1, line 50 - Col. 3, line 20).

Regarding claim 8, the Office Action suggests that Park discloses the method of claim 1 wherein said laminated structure includes a dielectric layer (40) below said gate conductor layer (50) a silicon layer below said gate dielectric layer (40), wherein said method further comprises a first doping process of doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process, wherein said method further comprises a second doping process of doping halo regions below said gate conductor in a self-aligned implantation with an impurity of an opposite polarity to that used in said first doping process after said first doping process, wherein the combined height of said gate conductor and said sacrificial layer prevents impurities from reaching said silicon layer, and whereas, without said sacrificial layer, said doping processes would implant impurities through said gate conductor and aid gate dielectric layer to said silicon layer (see Figs. 1-12 and related text Col. 1, line 50 - Col. 3, line 20).

Regarding claim 9, the Office Action suggests that Park discloses a method of forming an integrated circuit transistor having a reduced gate height, the method comprising: forming a laminated structure having a substrate (see Fig. 1), a gate conductor (50) above the substrate, and at least one sacrificial layer (54) above said gate conductor (see Fig. 1); patterning said laminated structure into at least one gat stack extending from said substrate; forming spacers with a target spacer width adjacent to the gate stack wherein in order to achieve the target spacer width, a combined height of the

gate conductor and the at least one sacrificial layer is predetermined; epitaxially growing raised source and drain regions on said substrate adjacent said gate stack (see Fig. 5); after said epitaxially growing of said raised source drain regions, implanting an impurity into said raised source and drain regions and into said substrate below the raised source drain regions (see Figs. 9 and 10); wherein implanting said impurity after said epitaxially growing and raised source drain regions avoids subjecting said impurities to the thermal budget of said epitaxially growing process and wherein said target spacer width is predetermined to ensure the spacers sufficiently separate the raised source drain regions form the gate stack so as to avoid lateral encroachment of the impurity unto a channel region below the gate stack regardless of a height of the gate conductor; and removing said spacers and said sacrificial layer (see Figs. 1-12 and related text Col. 1, line 50 - Col. 3, line 20).

Regarding claim 11, the Office Action suggests that Park discloses the method of claim 9 wherein the forming the spacers comprises forming of the spacers with target spacer width so as to positions said raised source and drain regions further from said gate conductor when compared to raised source and drain regions formed with spacers formed only to said height of said gate conductor (see Figs. 1-12 and related text Col. 1, line 50 - Col. 3, line 20).

Regarding claim 12, the Office Action suggests that Park discloses the method of claim 9 wherein said sacrificial layer above said gate conductor is formed in a process comprising: forming a sacrificial oxide layer above said gate conductor, and forming additional sacrificial layers above said oxide layer, wherein said sacrificial oxide layer

protects said gate conductor (see Figs. 1-12 and related text Col. 1, line 50 - Col. 3, line 20).

Regarding claim 13, the Office Action suggests that Park discloses the method of claim 9 wherein said laminated structure includes a gate dielectric (40) below said gate conductor layer and a silicon layer (i.e., part of SOI) below said gate conductor (50), wherein said method further comprises doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process, wherein the combined height of said gate conductor and said sacrificial layer prevents said impurity from reaching said silicon layer, and whereas, without said sacrificial layer, said doping process would implant an impurity through said gate conductor and said gate dielectric layer to said silicon layer (see Figs. 1-12 and related text Col. 1, line 50 - Col. 3, line 20).

Regarding claim 14, the Office Action suggests that Park discloses the method of claim 9 wherein said laminated structure includes a dielectric layer (40) below said gate conductor layer (50) a silicon layer below said gate dielectric layer (40), wherein said method further comprises a first doping process of doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process, wherein said method further comprises a second doping process of doping halo regions below said gate conductor in a self-aligned implantation with an impurity of an opposite polarity to that used in said first doping process after said first doping process, wherein the combined height of said gate conductor and said sacrificial layer prevents impurities from reaching said silicon layer, and whereas, without said sacrificial layer,

Appeal Brief

said doping processes would implant impurities through said gate conductor and aid gate dielectric layer to said silicon layer (see Figs. 1-12 and related text Col. 1, line 50 - Col. 3, line 20).

Regarding claim 15, the Office Action suggests that Park discloses the method of claim 9 wherein by implanting said impurity after said epitaxially growing process, said impurity avoid being diffused as result of said thermal budget of said epitaxially growing process (see Figs. 1-12 and related text Col. 1, line 50 - Col. 3, line 20).

Regarding claim 16, the Office Action suggests that Park discloses a method of forming an integrated circuit transistor having a reduced gate height, said method comprising: forming a laminated structure having a substrate, a gate conductor above said substrate, and at least one sacrificial layer above said gate conductor; patterning said laminated structure into at least one gate stack extending from said substrate; forming spacers with a target spacer width adjacent said gate stack, wherein in order to achieve the target spacer width, a combined height of the gate conductor and the at least one sacrificial layer is predetermined; epitaxially growing raised source and drain regions on said substrate adjacent said spacers, wherein said process of epitaxially growing said raised source and drain regions is performed in the absence of doping impurities; after said epitaxially growing of said raised source drain regions, implanting impurities into said raised source and drain regions and into said substrate below the raised source drain regions (see Figs. 9 and 10); wherein implanting said impurities after said epitaxially growing and raised source drain regions avoids subjecting said impurities to the thermal budget of said epitaxially growing process and wherein said target spacer width is

predetermined to ensure the spacers sufficiently separate the raised source drain regions form the gate stack so as to avoid lateral encroachment of the impurity unto a channel region below the gate stack regardless of a height of the gate conductor; and removing said spacers and said sacrificial layer (see Figs. 1-12 and related text Col. 1, line 50 - Col. 3, line 20).

Regarding claim 17, the Office Action suggests that Park discloses the method of claim 16 wherein forming of the spacers adjacent the gate stack comprises forming of the spacers adjacent the gate conductor and at least on sacrificial oxide layer (54) above the gate conductor (50) (see Figs. 1-12 and related text Col. 1, line 50 - Col. 3, line 20).

Regarding claim 19, the Office Action suggests that Park discloses the method of claim 16 wherein the forming the spacers comprise forming the spacers with target spacer so as to positions said source and drain regions further from said gate conductor when compared to source and drain regions formed with spacers formed only to said height of said gate conductor (see Figs. 1-12 and related text Col. 1, line 50 - Col. 3, line 20).

Regarding claim 20, the Office Action suggests that Park discloses the method of claim 16 wherein said sacrificial layer above said gate conductor is formed in a process comprising: forming a sacrificial oxide layer above said gate conductor, and forming additional sacrificial layers above said oxide layer (see Figs. 1-12 and related text Col. 1, line 50 - Col. 3, line 20).

Regarding claim 21, the Office Action suggests that Park discloses the method of claim 16 wherein said sacrificial oxide layer protects said gate conductor (see Figs. 1-12 and related text Col. 1, line 50 - Col. 3, line 20).

Appeal Brief

Regarding claim 22, the Office Action suggests that Park discloses the method of claim 16 wherein said laminated structure includes a gate dielectric (40) below said gate conductor layer and a silicon layer (i.e., part of SOI) below said gate conductor (50), wherein said method further comprises doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process, wherein the combined height of said gate conductor and said sacrificial layer prevents said impurity from reaching said silicon layer, and whereas, without said sacrificial layer, said doping process would implant an impurity through said gate conductor and said gate dielectric layer to said silicon layer (see Figs. 1-12 and related text Col. 1, line 50 - Col. 3, line 20).

Regarding claim 23, the Office Action suggests that Park discloses the method of claim 16 wherein said laminated structure includes a gate dielectric (40) below said gate conductor layer and a silicon layer below said gate dielectric layer, wherein said method further comprises a first doping process of doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process, wherein said method further comprises a second doping process of doping halo regions below said gate conductor in a self-aligned implantation with an impurity of an opposite polarity that used in said first doping process after said first doping process, wherein the combined height of said gate conductor and said sacrificial layer prevents impurities from reaching said silicon layer, and whereas, without said sacrificial layer, said doping processes would implant impurities through said gate conductor and gate dielectric layer to said silicon layer (see Figs. 1-12 and related text Col. 1, line 50 - Col. 3, line 20).

Appeal Brief

Regarding claim 24, the Office Action suggests that Park discloses a method of producing an integrated circuit transistor comprising: forming a laminated stack deposition, wherein said laminated stack deposition is formed in a process comprising: forming a silicon layer over a substrate layer (30) (i.e., part of SOI); forming a gate oxide (40) on said silicon layer (30); forming a gate conductor (50) on said gate oxide (40); and forming of least one sacrificial material above said gate conductor, patterning said gate oxide (see Figs. 5 and 6), gate conductor, and said sacrificial material into at least one gate stack (see Figs. 1-6); forming temporary spacers (70 60) with a target width adjacent said gate stack (55), wherein in order to achieve the target spacer width, a combined height of the gate conductor and the at least one sacrificial layer is predetermined; epitaxially growing raised source and drain regions (36) (see Fig. 6) above said substrate layer adjacent said temporary spacers, such that said temporary spacers separate said raised source and drain regions from said gate stack, wherein the epitaxially growing process of the raised source and drain regions performed in the absence of doping of impunties; simultaneously implanting impurities into said raised source and drain regions and into said substrate below the raised source drain regions (see Figs. 9 and 10); wherein implanting said impurities after said epitaxially growing and raised source drain regions avoids subjecting said impurities to the thermal budget of said epitaxially growing process and wherein said target spacer width is predetermined to ensure the spacers sufficiently separate the raised source drain regions form the gate stack so as to avoid lateral encroachment of the impurity into a channel region below the gate stack regardless of a height of the gate conductor; growing an additional dielectric layer (44) (see Fig. 8)

on said raised source and drain regions (36); removing said temporary spacers (see Fig. 9) without removing said sacrificial material (51); performing a halo implant (see Fig. 10) in said raised source and drain regions and in exposed regions of said silicon layer; forming a permanent spacer (80) (see Fig. 11) adjacent said gate stack, wherein said permanent spacer is thinner than said temporary spacer; performing a source and drain extensions implant in said raised source and drain regions and exposed regions of said silicon; forming a final spacer filling said exposed regions of said silicon between said permanent spacer and said raised source and drain regions; implanting additional impurity into said raised source and drain regions and exposed regions of said silicon; annealing to activate all impurity; etching back said additional dielectric layer on said raised source and drain regions; and saliciding both said gate conductor and said raised source and drain regions (see Figs. 1-12 and related text Col. 1, line 50 - Col. 3, line 20).

Regarding claim 26, the Office Action suggests that Park discloses the method of claim 24 wherein said removing of said sacrificial layer reduces the height of said gate conductor relative to the gate height associated with the spacing of the source and drain regions created by said spacers (see Figs. 1-12 and related text Col. 1, line 50 - Col. 3, line 20).

Regarding claim 27, the Office Action suggests that Park discloses the method of claim 24 wherein said forming of said sacrificial material above said gate conductor further comprises forming a sacrificial oxide layer above said gate conductor, forming a sacrificial nitride layer above said oxide layer and forming a sacrificial hard insulator material above said nitride layer (see Figs. 1-12 and related text Col. 1, line 50 - Col. 3,

Appeal Brief

line 20).

Regarding claim 28, the Office Action suggests that Park discloses the method of claim 24 wherein said sacrificial oxide layer protects said gate conductor (see Figs. 1-12 and related text Col. 1, line 50 - Col. 3, line 20).

C. The Appellants' Position Regarding The Prior Art Rejections Of Claims 1-2, 4-9, 11-17, 19-24, and 26-28

1. The Appellants' Position Regarding Independent Claims 1, 9, 16 and 24 Generally.

The Applicants respectfully traverse the rejection of the independent claims 1, 9, 16 and 24 and, their respective dependent claims, because Park does not teach or suggest several of the claimed features as required for a rejection under 35 U.S.C. §102(b). Specifically, regarding independent claims 1, 9, 16 and 24, Park does not teach or suggest the following features: (1) "forming spacers with a target spacer width adjacent to said gate stack, wherein in order to achieve said target spacer width a combined height of said gate conductor and said at least one sacrificial layer is predetermined" and (2) "wherein said target spacer width is predetermined to ensure that said spacers (or said temporary spacers, see claim 24) sufficiently separate said source and drain regions (or said raised source and drain regions, see claims 9, 16 and 24) from said gate stack so as to avoid lateral encroachment of said impurity into a channel region below said gate stack regardless of a height of said gate conductor." Regarding independent claims 9, 16 and

Appeal Brief

24, Park does not teach or suggest "after said epitaxially growing of said raised source and drain regions, implanting an impurity into said raised source and drain regions and into said substrate below said raised source and drain regions, wherein implanting said impurity after said epitaxially growing of said raised source and drain regions avoids subjecting said impurity to the thermal budget of said epitaxially growing process." Finally, regarding independent claims 16 and 24, Park also does not teach or suggest the feature "said process of epitaxially growing said raised source and drain regions is performed in the absence of doping impurities".

2. The Appellants' Position Regarding Independent Claims 1

Regarding independent claim 1Park does not teach or suggest the following features: (1) "forming spacers with a target spacer width adjacent to said gate stack, wherein in order to achieve said target spacer width a combined height of said gate conductor and said at least one sacrificial layer is predetermined" and (2) "wherein said target spacer width is predetermined to ensure that said spacers sufficiently separate said source and drain regions from said gate stack so as to avoid lateral encroachment of said impurity into a channel region below said gate stack regardless of a height of said gate conductor."

Park and the present invention each provide methods for forming CMOS transistors with raised source and drain regions; however, the problems addressed are different as are the processes used to solve the problems. The present invention addresses the problem of encroachment of source/drain dopants into the channel region when gate heights are scaled (see paragraph [0001]). That is, with increased scaling of

Appeal Brief

CMOS structures and, specifically, of gate heights, implanting dopants with sufficient energy to dope the source and drain regions and halos using the polygate as a self-aligned mask can cause the dopants to laterally diffuse through the substrate into the channel region as well as penetrate through the poly gate and the gate dielectric into the channel as the gate height is decreased (see paragraphs [0001-0006]). The maximum achievable size of the sidewall spacers is reduced due to the reduced step height for reactive ion etch of a deposited spacer material of a given thickness and, thus, the spacers may not be sufficiently wide enough to avoid lateral encroachment of S/D dopants (see paragraph [0005]). There is also a higher probability of silicide bridging between the gate and the S/D (see paragraph [0005]). This problem becomes more severe when using epitaxially grown raised source and drain structures because epitaxial overgrowth occurs on top of the gate with reduced height (see paragraph [0005]). The undesirably overgrown epitaxial polysilicon over the gate would also be silicided which would form a conductive path between the gate and the raised source/drain regions, resulting in failure of transistor function.

Therefore, as mentioned in paragraphs [0008-0010], [0030], [0036], [0039]) of the present application, the method of the invention forms a gate stack with a gate conductor and at least one sacrificial layer (see Figures 2A-2B). Spacers 60 are then formed with a target spacer width adjacent to that gate stack (see paragraph [0040] and Figures 6A-6B). The target spacer width is predetermined to ensure that the spacers sufficiently separate the source and drain regions from the gate stack so as to avoid lateral encroachment of the impurity into the channel region (see paragraphs [0008], [0029],

Appeal Brief

[0030]--which refers to the lateral encroachment problem discussed in paragraph [0005]), [0031], [0035-0036], [0039-0040] and [0050]). In order to achieve this target spacer width, regardless of the height of the gate conductor alone, the combined height of the gate conductor and the sacrificial layer(s) is predetermined (seeparagraphs [0008], [0029-0031], [0035-0036], [0039-0040] and [0050]) .

Contrarily, Park addresses the problem of unwanted overgrown epi growth on the gate and STI (see column 1, lines 10-18) but not the formation of spacers sufficiently large enough to avoid unwanted lateral diffusion of dopants into channel regions when gate heights are reduced. Specifically, Park discloses a method of forming CMOS transistors with raised source and drain regions (col. 1, lines 5-6). In the Park method a conventional gate stack is formed with several thin sacrificial layers 51, 52, 54 above the 120nm gate conductor 50 (see column 1, lines 58-62 and Figure 1). These sacrificial layers protect the surface of the gate conductor during subsequent processing.

A protective nitride layer 60 is deposited over the substrate and the gate-sacrificial layers (see column 1, lines 66-67 and Figure 2. Then, temporary spacers 70 are formed on the protective nitride layer 60 against the gate stack and a width of these temporary spacers 70 is "set to define the area for the halo and extensions implants" (see column 2, lines 1-5). A portion of the protective layer 60 above the substrate is etched to define the area for implant of the source and drain regions and then, the temporary spacers 70 are removed (see column 2, lines 25-30). Then, the source and drain regions 34 are implanted, although this step can be omitted if the source and drain regions were previously implanted (see column 2, lines 33-34 and Figure 5). Column 2, lines 34-37

provide that "the layer 60 is thick enough to block the implant in the region that will contain the extension implant." After the source and drain regions 34 are implanted in the substrate, raised source and drain regions 36 are epitaxially grown (see column 2, lines 43-47 and Figure 7). Unwanted epi growth is prevented by the remaining nitride layer 60 on the gate stack and adjacent to the gate stack in the area of the substrate designated for the S/D extension. Then, after additional processing steps, extension and halo implantation is performed (see column 2, lines 48-64), which also implants the raised epitaxially grown source and drain regions 36.

Park does not address the issue of lateral encroachment of the impurities (i.e., dopants) from the source and drain regions 34 into the channel because the Park transistor does not have a reduced gate height (it has a nominal gate height of 120nm (see column 1, line 59) and, thus, the ability to form spacers with a width sufficient enough to avoid lateral encroachment of the dopants into the channel region was not a problem for Park. Specifically, Park mentions that the widths of the spacers 70 that are formed adjacent to the gate conductor are "set to define the area for the halo and extensions implants" (see column 2, lines 1-5). Park also indicates that the nitride layer 60 is thick enough to block penetration by the source/drain dopant through the nitride layer down into the area of the substrate designated for the halo and extensions implants (col. 2, lines 34-37) and further discusses the protection provided by sacrificial layers 51, 52 and 54 during subsequent processing. However, the Park gate conductor was disclosed as nominally 120nm thick (see col. 1, lines 57-60) and, thus, those skilled in the art will recognize the gate height was sufficiently tall to achieve spacers with the required target spacer width. Therefore,

an alternative technique for achieving the target spacer width was not needed, considered or disclosed.

More specifically, regarding independent claim 1, Park does not teach or suggest "forming spacers with a target spacer width adjacent to said gate stack, wherein in order to achieve said target spacer width a combined height of said gate conductor and said at least one sacrificial layer is predetermined" or "wherein said target spacer width is predetermined to ensure that said spacers sufficiently separate said source and drain regions from said gate stack so as to avoid lateral encroachment of said impurity into a channel region below said gate stack regardless of a height of said gate conductor."

Given the conventional gate height of 120nm disclosed in Park, spacers 70 the maximum achievable spacer height was necessarily sufficient to separate the source and drain regions 34 from the gate stack and, thereby, avoid lateral encroachment of the S/D impurities into the channel region without additional processing. Lateral encroachment is only avoided in Park because the height of the gate conductor was not reduced and, thus, was sufficiently tall to produce spacers with the necessary width.

On page 12 the Office Action specifically suggests that Figure 5 depicts that "the S/D implantation process occurs in the presences of oxide liner 42 and nitride spacer 60 that is sufficient to avoid *encroachment of said impurity into a channel region.* Page 12 of the Office Action further indicates that Figures 2 and 3 depict that "the sacrificial spacer 70 and of oxide liner 42 and nitride spacer 60 (i.e., the target spacers) have a combined predetermined height and width. In addition, the spacers have predetermined thickness and height that ensures that sufficient separation during that source and drain

regions formation so that lateral encroachment of said impurity into a channel region below said gate stack regardless of a height of said gate conductor could be avoided." Finally, page 12 of the Office Action suggests that Park discloses "forming the target spacer" in Figures 1-5. Specifically, it states that "the target spacers (42, 60, 70) are formed to protect the gate electrode and the channel region under the gate electrode during amorphization ion implant process (see Figs. 2 and 3) prior implanting the S/D implant. In Addition, none the drawing shown diffusion of the impurities under the gate conductor (i.e., in the channel region) as shown in Figs. 5-8. As shown Fig. 5, the target spacer protects the channel region for impurities during the S/D implantation process. In addition, it is respectfully submitted that the lateral encroachment never occur in Park et. al. '084 disclosure because the use of spacer as well dummy spacer is intended to avoid such problem. This is the art-recognized problem so that Park et al. '084 process also intended to avoid such a problem." The Applicants respectfully disagree.

Figure 5 of Park shows the existence of an oxide liner 42 and nitride spacer 60, it does not show that the liner 42/spacer 60 are sufficient to avoid encroachment (and particularly lateral encroachment) of an impurity into a channel region. The fact that Figure 5 does not illustrate impurities under the gate conductor is irrelevant because the gate height of Park is not reduced and, so lateral encroachment did not need to be considered. Additionally, support for the fact that lateral diffusion of dopants was not considered by Park is found in the fact that not only does Figure 5 fail to show lateral diffusion of impurities into the channel region but also fails to show any lateral diffusion of impurities at all. Those skilled in the art would recognize that such lateral diffusion

would necessarily occur to some extent, especially following the epi growth process in Park. Thus, in Park the absence of an illustration which shows lateral dopant diffusion only supports the fact that lateral diffusion was not an issue. It does not support a finding that Park disclosed that the combined height of the gate stack was predetermined so that spacers with a predetermined target spacer width could be achieved in order to avoid lateral encroachment of the source and drain impurities into the channel region.

Furthermore, Figures 2 and 3 of Park show that the sacrificial spacer 70, oxide liner 42 and nitride spacer 60 necessarily have a combined height (which may or may not be predetermined. However, these Figures do not show that the "target spacer width (i.e., the width of spacer 60) is predetermined to ensure that said spacers (or said temporary spacers, see claim 24) sufficiently separate said source and drain regions (or said raised source and drain regions, see claims 9, 16 and 24) from said gate stack so as to avoid lateral encroachment of said impurity into a channel region below said gate stack regardless of a height of said gate conductor". Park only mentions that the widths of the spacers that are formed adjacent to the gate conductor are "set to define the area for the halo and extensions implants" (see column 2, lines 1-5). It does not disclose any other details regarding the width of the spacers.

In view of the foregoing, the Appellants respectfully submit that the Park does not teach or suggest the features defined by independent claim 1. Further, dependent claims 2 and 4-8 are similarly patentable over, not only by virtue of their dependency from patentable independent claims, respectively, but also by virtue of the additional features of the Appellants' claimed invention they define.

Appeal Brief

3. The Appellants' Position Regarding Independent Claim 9

Regarding independent claim 9, Park does not teach or suggest the following features: (1) "forming spacers with a target spacer width adjacent to said gate stack, wherein in order to achieve said target spacer width a combined height of said gate conductor and said at least one sacrificial layer is predetermined"; (2) "wherein said target spacer width is predetermined to ensure that said spacers sufficiently separate said raised source and drain regions from said gate stack so as to avoid lateral encroachment of said impurity into a channel region below said gate stack regardless of a height of said gate conductor."; and (3) "after said epitaxially growing of said raised source and drain regions, implanting an impurity into said raised source and drain regions and into said substrate below said raised source and drain regions, wherein implanting said impurity after said epitaxially growing of said raised source and drain regions avoids subjecting said impurity to the thermal budget of said epitaxially growing process."

Features (1) and (2) of claim 9 are similar to the features of claim 1 addressed in paragraph 2 above and are similarly patentable.

Furthermore, Park also does not teach or suggest feature (4) of "after said epitaxially growing of said raised source and drain regions, implanting an impurity into said raised source and drain regions and into said substrate below said raised source and drain regions, wherein implanting said impurity after said epitaxially growing of said raised source and drain regions avoids subjecting said impurity to the thermal budget of said epitaxially growing process" (see paragraphs [0042] and [0047]). Specifically, Park discloses implanting the source and drain regions 34 in the substrate *before growing the*

epi for the raised source/drain regions 36 (see column 2, lines 33-48 and see Figure 5). The impurities implanted into these source and drain regions 34 in the substrate would necessarily be subjected to the epi process (column 2, lines 44-48 and see Figure 7) with a conventional temperature range from about 750°C-850°C and, thus, subjected to the deleterious effects of transient enhanced diffusion of impurities, such as boron.

Page 13 of the Office Action cites Figures 9 and 10 as disclosing that the implant to form the S/D extension is conducted after the epitaxial layer is formed. Specifically, it indicates that "[T]he implant form S/D extension is conducted after the epitaxial layer formed (see Figs. 9 and 10). Furthermore, the impurities 35' below the epi-layer 36 (see Fig. 10) is occurred due to the implantation process after the epitaxial layer 36 is formed and does not required any heating (annealing) process to diffuse the dopant into the epitaxial layer 36, as shown in Fig. 10 (i.e., wherein implanting the impurities after epitaxially growing the raised source and drain regions avoids subjecting the impurities to the thermal budget of the epitaxially grown." The Applicants respectfully disagree.

The S/D extension 35 in Figures 9 and 10 of Park is not the same as the source/drain regions 34 (see labeling in Figures 5-7). Specifically, col. 2, lines 34-40 of Park disclose the implant of source/drain regions 34 in the substrate adjacent to that region of the substrate that is blocked by nitride 60 and defines the area of the substrate that will contain the extension. After the source/drain regions 34 are implanted into the substrate, the epi process is performed (see col. 2, lines 40-48) and the dopants in the source/drain regions are necessarily subjected to the thermal epi process resulting in diffusion of the s/d dopants. Col. 2, lines 56-58 and associated Figures 9-10 simply

disclose that after the epi is grown, a thermal oxide layer is grown on the epi (Figure 9) and a second implant process is used to implant the halos and extensions (Figure 10) to avoid subjecting the halos/extensions to the thermal epi process. Specifically, after the raised source/drain regions 36 are eptiaxially grown on the doped regions 34 in the substrate in Park, regions 35 and 37 are implanted into the substrate in an area immediately adjacent to the previously doped regions 34 (not into the substrate below the epi layer 36) and regions 35' and 37' are implanted into the raised s/d epi regions 36 (not into the doped s/d regions 34 below the epi layer 36, as suggested)(see Figures 5, 9-10 and the associated text in the specification of Park). Thus, in Park impurities are not simultaneously implanted into both the raised source and drain regions and into the substrate below the raised source and drain regions (see claims 9 and 24 of the present invention). Additionally, the doped source/drain regions 34 of Figure 5 are necessarily subjected to the thermal budgeting of the epi growth process at Figure 7. Again, the source/drain regions 34 of Park that are *below* the raised source/drain regions 36 of Figures 9-10 of Park were doped prior to the epi process (see Figure 5).

In view of the foregoing, the Appellants respectfully submit that the Park does not teach or suggest the features defined by independent claim 9. Further, dependent claims 11-15 are similarly patentable over, not only by virtue of their dependency from patentable independent claims, respectively, but also by virtue of the additional features of the Appellants' claimed invention they define.

4. The Appellants' Position Regarding Independent Claims 16 and 24

Appeal Brief

Regarding independent claims 16 and 24 Park does not teach or suggest the following features: (1) "forming spacers with a target spacer width adjacent to said gate stack, wherein in order to achieve said target spacer width a combined height of said gate conductor and said at least one sacrificial layer is predetermined"; (2) "wherein said target spacer width is predetermined to ensure that said spacers (or said temporary spacers, see claim 24) sufficiently separate said raised source and drain regions from said gate stack so as to avoid lateral encroachment of said impurity into a channel region below said gate stack regardless of a height of said gate conductor"; (3) "after said epitaxially growing of said raised source and drain regions, implanting an impurity into said raised source and drain regions and into said substrate below said raised source and drain regions, wherein implanting said impurity after said epitaxially growing of said raised source and drain regions avoids subjecting said impurity to the thermal budget of said epitaxially growing process"; and (4) "said process of epitaxially growing said raised source and drain regions is performed in the absence of doping impurities".

Features (1) and (2) of claims 16 and 24 are similar to the features of claim 1 addressed in paragraph 2 above and are similarly patentable. Additionally, feature (3) of claims 16 and 24 is similar to the feature of claim 9 addressed in paragraph 3 above and is similarly patentable.

Furthermore, Park does not teach feature (4) of "said process of epitaxially growing said raised source and drain regions is performed in the absence of doping impurities." The Office Action cites Figures 9 and 10 as teaching this feature. However, as mentioned above, Park teaches doping the source and drain regions 34 in the substrate

prior to growing the epi on those source and drain regions (see Figures 5-7 and associated text in the Specification). Thus, Park necessarily teaches that the process of epitaxially growing the raised source and drain regions 36 is performed in the presence, not the absence, of doping impurities.

In view of the foregoing, the Appellants respectfully submit that the Park does not teach or suggest the features defined by independent claims 16 and 24. Furthermore, dependent claims 17, 19-23 and 26-28 are similarly patentable over, not only by virtue of their dependency from patentable independent claims, respectively, but also by virtue of the additional features of the Appellants' claimed invention they define.

5. The Appellants' Final Position Regarding Independent Claims 1, 9, 16 and 24

MPEP §2131 provides guidance regarding 35 U.S.C. §102 Anticipation rejections and specifically states that "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." See *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). It further states that "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). In light of the above, the Applicants respectfully submit that each and every element has not been disclosed by Park and, more particularly, that the identical invention is not shown in as complete detail as contained in the claims. Therefore, the Applicants respectfully submit that independent claims 1, 9, 16, and 24 are patentable over the prior art of record.

Appeal Brief

Furthermore, the Applicants submit that dependent claims 4-8, 11-15, 17, 19-23 and 26-28 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view of the foregoing, the Board is respectfully requested to reconsider and withdraw the rejections.

VIII. CONCLUSION

In view of the foregoing, the Appellants respectfully submit that the Park does not teach or suggest the features defined by independent claims 1, 9, 16, and 24, and as such, claims 1, 9, 16, and 24 are patentable over PArk. Furthermore, dependent claims 2, 4-8, 11-15, 17, 19-23, and 26-28 are similarly patentable over, not only by virtue of their dependency from patentable independent claims, respectively, but also by virtue of the additional features of the Appellants' claimed invention they define. Thus, the Appellants respectfully request that the Board reconsider and withdraw the rejections of claims 1-2, 4-9, 11-17, 19-24, and 26-28 and pass these claims to issue.

Appeal Brief

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0458.

Respectfully submitted,

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IX. CLAIMS APPENDIX

1. A method of forming an integrated circuit transistor having a reduced gate height, said method comprising:

forming a laminated structure having a substrate, a gate conductor above said substrate, and at least one sacrificial layer above said gate conductor;

patterning said laminated structure into at least one gate stack extending from said substrate;

forming spacers with a target spacer width adjacent to said gate stack, wherein in order to achieve said target spacer width, a combined height of said gate conductor and said at least one sacrificial layer is predetermined;

doping regions of said substrate not protected by said spacers with an impurity to form source and drain regions adjacent said gate stack, wherein said target spacer width is predetermined to ensure that said spacers sufficiently separate said source and drain regions from said gate stack so as to avoid lateral encroachment of said impurity into a channel region below said gate stack regardless of a height of said gate conductor; and

removing said spacers and said sacrificial layer.

2. The method in claim 1, wherein said forming of said spacers adjacent said gate stack comprises forming said spacers adjacent said gate conductor and said at least one sacrificial oxide layer above said gate conductor.

Appeal Brief

3. (Cancelled).

4. The method in claim 1, wherein said forming of said spacers comprises forming said spacers so as to positions said source and drain regions further from said gate conductor when compared to source and drain regions formed with spacers formed only to said height of said gate conductor.

5. The method in claim 1, wherein said sacrificial layer above said gate conductor is formed in a process comprising:

forming a sacrificial oxide layer above said gate conductor, and

forming additional sacrificial layers above said oxide layer.

6. The method in claim 5, wherein said sacrificial oxide layer protects said gate conductor.

7. The method in claim 1, wherein said laminated structure includes a gate dielectric layer below said gate conductor layer and a silicon layer below said gate dielectric layer,

wherein said method further comprises doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process,

wherein the combined height of said gate conductor and said sacrificial layer prevents said impurity from reaching said silicon layer, and

whereas, without said sacrificial layer, said doping process would implant said

impurity through said gate conductor and said gate dielectric layer to said silicon layer.

8. The method in claim 1, wherein said laminated structure includes a gate dielectric layer below said gate conductor layer and a silicon layer below said gate dielectric layer,

wherein said method further comprises a first doping process of doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process,

wherein said method further comprises a second doping process of doping halo regions below said gate conductor in a self-aligned implantation with an impurity of an opposite polarity to that used in said first doping process after said first doping process,

wherein the combined height of said gate conductor and said sacrificial layer prevents impurities from reaching said silicon layer, and

whereas, without said sacrificial layer, said doping processes would implant impurities through said gate conductor and said gate dielectric layer to said silicon layer.

9. A method of forming an integrated circuit transistor having a reduced gate height, said method comprising:

forming a laminated structure having a substrate, a gate conductor above said substrate, and at least one sacrificial layer above said gate conductor;

patterning said laminated structure into at least one gate stack extending from said substrate;

forming spacers with a target spacer width adjacent to said gate, wherein in order

to achieve said target spacer width, a combined height of said gate conductor and said at least one sacrificial layer is predetermined;

epitaxially growing raised source and drain regions on said substrate adjacent said spacers;

after said epitaxially growing of said raised source and drain regions, implanting an impurity into said raised source and drain regions and into said substrate below said raised source and drain regions,

wherein implanting said impurity after said epitaxially growing of said raised source and drain regions avoids subjecting said impurity to the thermal budget of said epitaxially growing process and wherein said target spacer width is predetermined to ensure that said spacers sufficiently separate said raised source and drain regions from said gate stack so as to avoid lateral encroachment of said impurity into a channel region below said gate stack regardless of a height of said gate conductor; and

removing said spacers and said sacrificial layer.

10. (Cancelled).

11. The method in claim 9, wherein said forming of said spacers comprises forming said spacers with said target spacer width so as to positions said raised source and drain regions further from said gate conductor when compared to raised source and drain regions formed with spacers formed only to said height of said gate conductor.

Appeal Brief

12. The method in claim 9, wherein said sacrificial layer above said gate conductor is formed in a process comprising:

forming a sacrificial oxide layer above said gate conductor, and

forming additional sacrificial layers above said oxide layer,

wherein said sacrificial oxide layer protects said gate conductor.

13. The method in claim 9, wherein said laminated structure includes a gate dielectric layer below said gate conductor layer and a silicon layer below said gate dielectric layer,

wherein said method further comprises doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process,

wherein the combined height of said gate conductor and said sacrificial layer prevents said impurity from reaching said silicon layer, and

whereas, without said sacrificial layer, said doping process would implant said impurity through said gate conductor and said gate dielectric layer to said silicon layer.

14. The method in claim 9, wherein said laminated structure includes a gate dielectric layer below said gate conductor layer and a silicon layer below said gate dielectric layer,

wherein said method further comprises a first doping process of doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process,

wherein said method further comprises a second doping process of doping halo regions below said gate conductor in a self-aligned implantation with an impurity of an

opposite polarity to that used in said first doping process after said first doping process,

wherein the combined height of said gate conductor and said sacrificial layer prevents impurities from reaching said silicon layer, and

whereas, without said sacrificial layer, said doping processes would implant impurities through said gate conductor and said gate dielectric layer to said silicon layer.

15. The method in claim 9, wherein by implanting said impurity after said epitaxially growing process, said impurity avoids being diffused as a result of said thermal budget of said epitaxially growing process.

16. A method of forming an integrated circuit transistor having a reduced gate height, said method comprising:

forming a laminated structure having a substrate, a gate conductor above said substrate, and at least one sacrificial layer above said gate conductor;

patterning said laminated structure into at least one gate stack extending from said substrate;

forming spacers with a target spacer width adjacent to said gate stack, wherein in order to achieve said target spacer width, a combined height of said gate conductor and said at least one sacrificial layer is predetermined;

epitaxially growing raised source and drain regions on said substrate adjacent said spacers, wherein said process of epitaxially growing said raised source and drain regions is performed in the absence of doping impurities;

after said epitaxially growing of said raised source and drain regions, implanting an impurity into said raised source and drain regions and into said substrate below said raised source and drain regions,

wherein implanting said impurity after said epitaxially growing of said raised source and drain regions avoids subjecting said impurity to the thermal budget of said epitaxially growing process and wherein said target spacer width is predetermined to ensure that said spacers sufficiently separate said raised source and drain regions from said gate stack so as to avoid lateral encroachment of said impurity into a channel region below said gate stack regardless of a height of said gate conductor; and

removing said spacers and said sacrificial layer.

17. The method in claim 16, wherein said forming of said spacers adjacent said gate stack comprises forming said spacers adjacent said gate conductor and said at least one sacrificial oxide layer above said gate conductor.

18. (Cancelled).

19. The method in claim 16, wherein said forming of said spacers comprises forming said spacers with said target spacer width so as to positions said source and drain regions further from said gate conductor when compared to source and drain regions formed with spacers formed only to said height of said gate conductor.

Appeal Brief

20. The method in claim 16, wherein said sacrificial layer above said gate conductor is formed in a process comprising:

forming a sacrificial oxide layer above said gate conductor, and

forming additional sacrificial layers above said oxide layer.

21. The method in claim 20, wherein said sacrificial oxide layer protects said gate conductor.

22. The method in claim 16, wherein said laminated structure includes a gate dielectric layer below said gate conductor layer and a silicon layer below said gate dielectric layer,

wherein said method further comprises doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process,

wherein the combined height of said gate conductor and said sacrificial layer prevents said impurity from reaching said silicon layer, and

whereas, without said sacrificial layer, said doping process would implant said impurity through said gate conductor and said gate dielectric layer to said silicon layer.

23. The method in claim 16, wherein said laminated structure includes a gate dielectric layer below said gate conductor layer and a silicon layer below said gate dielectric layer,

wherein said method further comprises a first doping process of doping said

source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process,

wherein said method further comprises a second doping process of doping halo regions below said gate conductor in a self-aligned implantation with an impurity of an opposite polarity to that used in said first doping process after said first doping process,

wherein the combined height of said gate conductor and said sacrificial layer prevents impurities from reaching said silicon layer, and

whereas, without said sacrificial layer, said doping processes would implant impurities through said gate conductor and said gate dielectric layer to said silicon layer.

24. A method of producing an integrated circuit transistor comprising:

forming a laminated stack deposition,

wherein said laminated stack deposition is formed in a process comprising:

forming a silicon layer over a substrate layer;

forming a gate oxide on said silicon layer;

forming a gate conductor on said gate oxide; and

forming of least one sacrificial material above said gate conductor,

patterning said gate oxide, gate conductor, and said sacrificial material into at least one gate stack;

forming temporary spacers with a target spacer width adjacent to said gate stack, wherein in order to achieve said target spacer width, a combined height of said gate conductor and said at least one sacrificial layer is predetermined;

epitaxially growing raised source and drain regions above said substrate layer adjacent said temporary spacers, such that said temporary spacers separate said raised source and drain regions from said gate stack, wherein said process of epitaxially growing said raised source and drain regions is performed in the absence of doping impurities;

simultaneously implanting an impurity into said raised source and drain regions and into said substrate below said raised source and drain regions,

wherein implanting said impurity after said epitaxially growing of said raised source and drain regions avoids subjecting said impurity to the thermal budget of said epitaxially growing process and wherein said target spacer width is predetermined to ensure that said temporary spacers sufficiently separate said raised source and drain regions from said gate stack so as to avoid lateral encroachment of said impurity into a channel region below said gate stack regardless of a height of said gate conductor;

growing an additional dielectric layer on said raised source and drain regions;

removing said temporary spacers without removing all of said sacrificial material;

performing a halo implant in said raised source and drain regions and in exposed regions of said silicon layer;

forming a permanent spacer adjacent said gate stack, wherein said permanent spacer is thinner than said temporary spacer;

performing a source and drain extensions implant in said raised source and drain regions and exposed regions of said silicon;

forming a final spacer filling said exposed regions of said silicon between said

permanent spacer and said raised source and drain regions;

implanting additional impurities into said raised source and drain regions and exposed regions of said silicon;

annealing to activate all impurities;

etching back said additional dielectric layer on said raised source and drain regions; and

saliciding both said gate conductor and said raised source and drain regions.

25. (Cancelled).

26. The method in claim 24, wherein said removing of said sacrificial layer reduces the height of said gate conductor relative to the gate height associated with the spacing of the source and drain regions created by said spacers.

27. The method in claim 24, wherein said forming of said sacrificial material above said gate conductor further comprises forming a sacrificial oxide layer above said gate conductor, forming a sacrificial nitride layer above said oxide layer and forming a sacrificial hard insulator material above said nitride layer.

28. The method in claim 24, wherein said sacrificial oxide layer protects said gate conductor.

X. EVIDENCE APPENDIX

There is no other evidence known to Appellants, Appellants' legal representative or Assignee which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

XI. RELATED PROCEEDINGS APPENDIX

There is no other related proceedings known to Appellants, Appellants' legal representative or Assignee which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.